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TECHNICAL NOTE

SEMI E-78

Method to Evaluate Semiconductor Processing Equipment for Static Charge

SEMI E-78 was developed to provide a consistent method to evaluate semiconductor processing equipment for static charge. Control of static charge is critical to reduce electrostatic discharge (ESD), electrostatic attraction (ESA) of contamination, and equipment discharge (resulting in equipment lock-up and/or damage) issues. The document is made up of 14 pages of requirements, an appendix, and four "related information" sections. These "related information" sections include some basics of electrostatics, static control, and interestingly one section that gives language to include in a semiconductor equipment purchasing document. Requirements from customers to Original Equipment Manufacturers (OEM's) have included a requirement for OEM's to obtain data that "proves" that the equipment meets the requirements in E-78 during equipment buyoff during the purchasing process. While compliance to E-78 is optional (per the standard), a customer can include compliance as a requirement for acceptance of a tool. In other cases, an OEM may choose to proactively test and show that their tools meet the requirements in E-78.

E78-0912 specifies the measurement of generated charge (nanoCoulombs) and electric field (volts/cm or volts/inch). Based on these measurements, E78-0912 assigns compliance levels based on technology nodes from the International Technology Roadmap for Semiconductors. Two categories are specified. They are:

1. ESD damage (to a product, wafer or reticle)
2. Particle attraction

Technology nodes are based on device sizes.

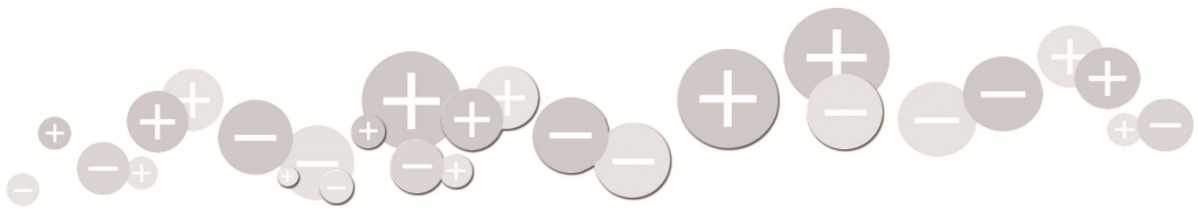
The latest revision (0912) of E-78 defines allowable charge levels on processing equipment and product as it is processed based on technology node. The table below, out of SEMI E-78, contains this data.

Based on this table, the history and development of which is covered in the Appendix of E-78, the projection continues for technology nodes to be increasingly smaller as time goes by. This table will likely be updated beyond 2023 with the next release.

In many cases a third-party consultant is employed to perform the E-78 assessment, as the equipment and skill required to perform an assessment is something many OEM's don't have in-house.

Equipment used for an assessment would include electrostatic field meters, resistance meters, and a nanoCoulomb meter with a Faraday Cup.

An E-78 assessment involves testing a semiconductor processing tool including the handling system that feeds the tool with wafers, as well as removing the wafer from the processing tool. However, it doesn't typically include the FOUP that is used to transport wafers between tools.



Year/Node	Wafers and Reticles Electrostatic Discharge (nC)	10 pF Device Electrostatic Discharge (nC)	10 pF Packaged Device Electrostatic Discharge (V)	Electrostatic Field		
				V/cm	V/m	(V/inch)
2000/180 nm	10.0	2.5-10	250-1000	200	20,000	(500)
2004/90 nm	10.0	1.0	100	100	10,000	(250)
2010/45 nm	2.5	0.25	25	50	5,000	(125)
2011/36 nm	1.8	0.18	18	41	4,100	(105)
2013/28 nm	1.1	0.11	11	31	3,100	(78)
2015/23 nm	0.74	0.074	7.4	26	2,600	(65)
2017/17.9 nm	0.45	0.045	4.5	20	2,000	(50)
2019/14.2 nm	0.27	0.027	2.7	16	1,600	(41)
2021/11.3 nm	0.18	0.018	1.8	12	1,200	(30)
2023/8.9 nm	0.12	0.012	1.2	8.9	890	(23)

Measurements that are made during the assessment to evaluate the electrostatic field (focusing on particle attraction mitigation) include verification of the grounding system and that all metal items in the tool are grounded. Other measurements include electrostatic field measurements of surfaces within the tool using an electrostatic field meter. This testing must be engineered so that the surfaces and wafer would be charged as it would be in the processing either while the tool is operating, or after it has been running for at least 2 hours. Another critical measurement for the ESD mitigation portion of the evaluation is evaluating the charge on a bare silicon wafer that is run through the process. In this case, the total charge on the wafer is measured using a large (very large for 300mm wafers) Faraday Cup. The goal of this part of the testing is to predict as accurately as possible specific tool performance as it relates to electrostatic control in the production environment.

To understand the testing process, an example of a SEMI E-78 assessment is described. Figure 1 is a hypothetical semiconductor processing tool. It represents a CVD module with two load locks and a minienvironment that processes the wafers in and out of the load locks.

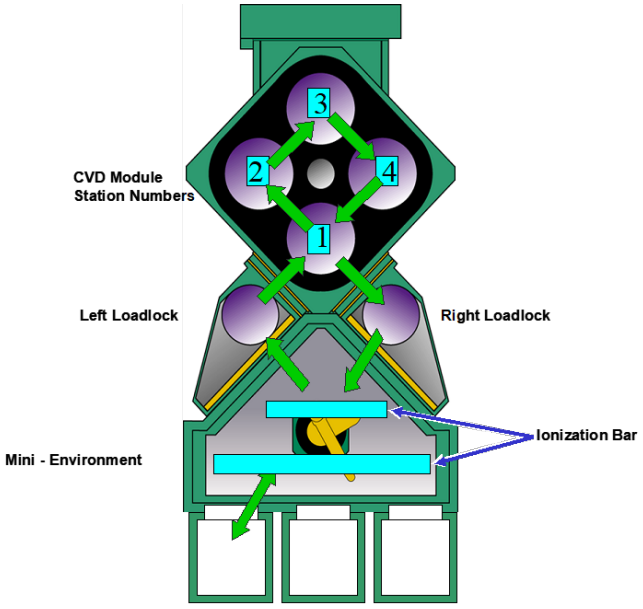


Figure 1

Particle Attraction Mitigation

Electrostatic Field Measurements

The E-78 evaluation would include having the tool run for an extended period of time (at least 2 hours), as it would normally operate (with ionization running, if installed). The tool would then be stopped, and the ionizers turned off to avoid having them impact the electrostatic fieldmeter/voltmeter measurements. Using care to avoid touching any of the surfaces, measurements of the various surfaces inside the tool, including wafer contact surfaces (where practical) would be made.

Electrostatic Discharge Mitigation

Wafer Charge Level Measurements

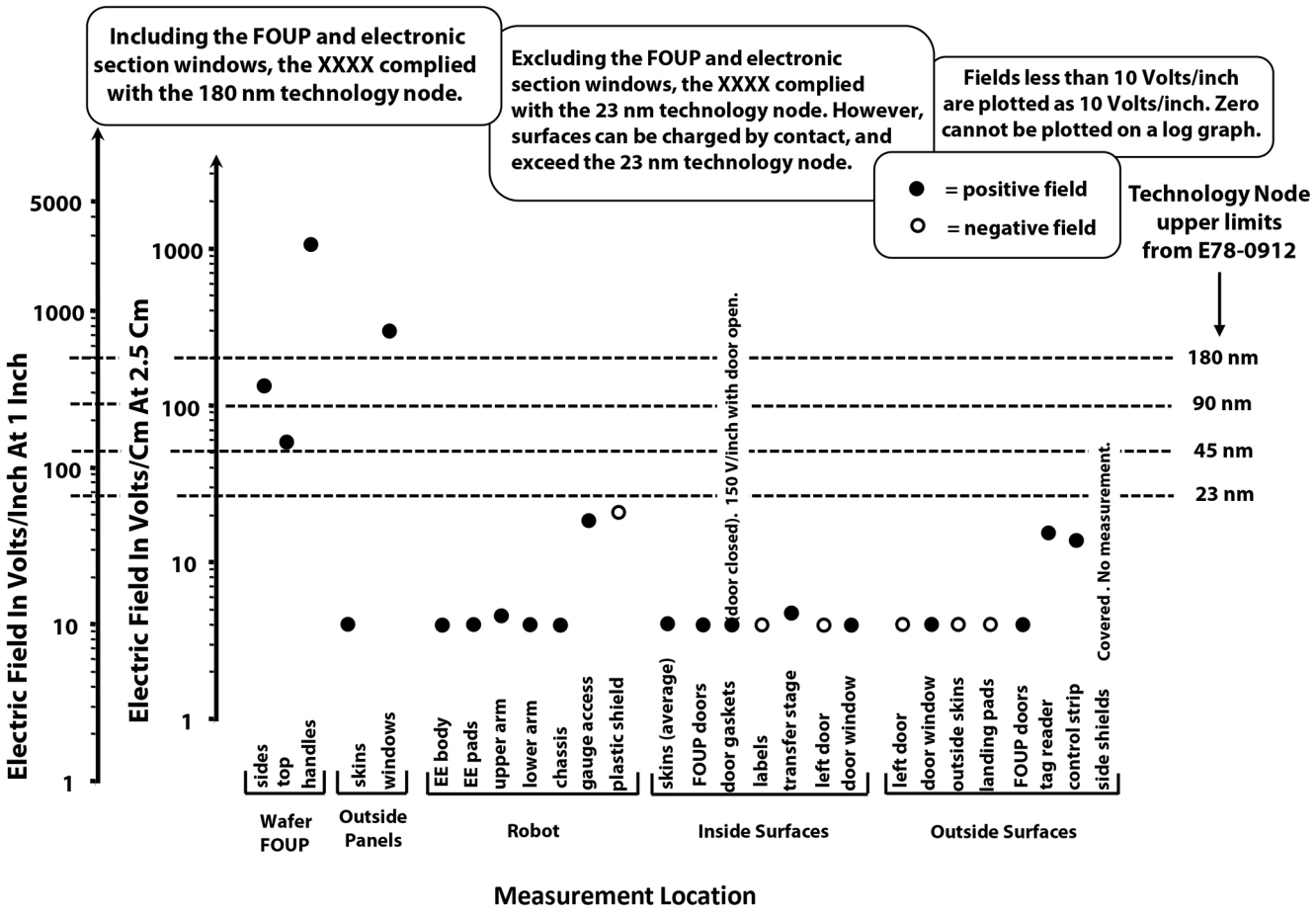
This measurement would involve processing a bare silicon wafer through the process, and then carefully measuring the total charge on the wafer using a large Faraday Cup, a nanoCoulomb meter and a custom-designed vacuum wand. Multiple tests are necessary to evaluate the statistical variability of the test. In addition, background tests are done to ensure that only charge applied to the wafer by the tool is measured (charge can be put on the wafer during handling for the test, which needs to be understood and subtracted from the total charge).

Evaluation of Results

The total charge on the wafer, and the electrostatic fields present in the tool are then compared to the data table in E-78 to determine the compatibility of the tool to a certain technology node. If needed, additional ionization, grounding, or modification of tool processing/materials may be required to make a tool compatible with the intended processing technology node.

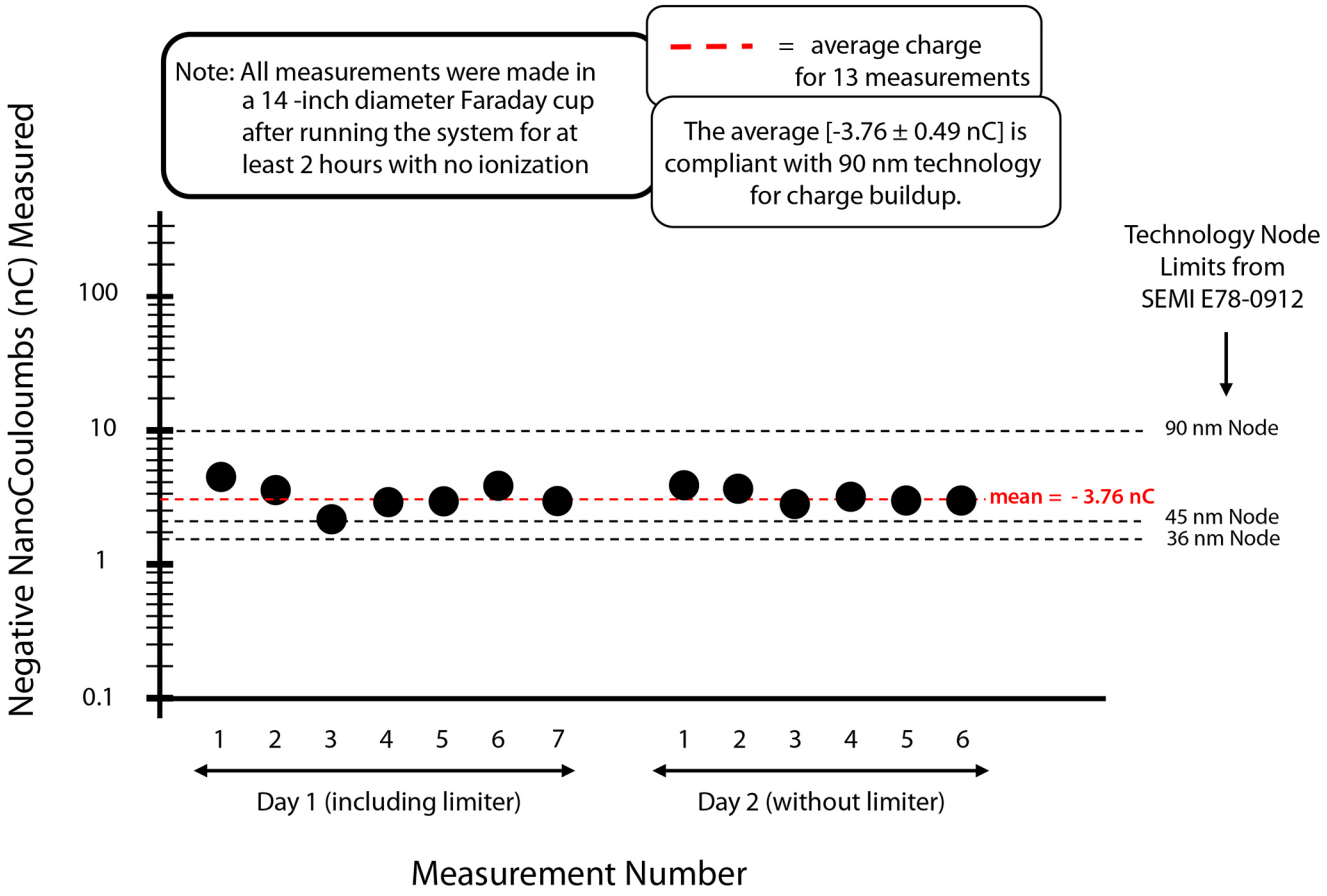
As an example of the tool being evaluated, after running the tool as described above, measurements were made and most of the electrostatic fields were found to be below 30 volts/inch (11.3 nm technology node. Several readings were found above the 23 nm technology node, the first three were the FOUP, which were ignored. The outside window panel was an issue that was highlighted by the E-78 evaluation and was addressed. See Figure 2.

Figure 2. Electric Field for Hypothetical Tool vs. Technology Node (from E78-0912)



In addition, after measuring several wafers after processing through the tool, it was found that the average charge on the wafer was found to be -3.76 nC. See Figure 3.

Figure 3. Charge Build-up Due to One Pass of a Bare Silicon Wafer Through the Tool



Comparing this data to the table from E-78-0912, we can see that the tool would meet the requirements for 23 nm technology for ESA (Particle Attraction), and 90 nm technology for ESD (Electrostatic Discharge).

Concerns about E-78

The testing defined in E-78, does not take into account many critical items that should be considered when evaluating a tool (or toolset). Different wafer materials, processing tools, ionizer configurations etc. can give widely differing results. Details on these issues are covered in a separate Technical Note.

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